CLAIMS

What is claimed is:

1. A binary hysteresis circuit, comprising:

first and second multi-bit circuit input terminals;

a comparator circuit having a first multi-bit input terminal, a second multi-bit input terminal coupled to the second circuit input terminal, and an output terminal;

a multiplexer circuit having a first data input terminal coupled to the first circuit input terminal, a second data input terminal, a select terminal coupled to the output terminal of the comparator circuit, and an output terminal coupled to the first input terminal of the comparator circuit; and

a first adder circuit coupled between the first circuit input terminal and the second data input terminal of the multiplexer circuit.

2. The binary hysteresis circuit of Claim 1, further comprising a second adder circuit coupled between the first circuit input terminal and the first data input terminal of the multiplexer circuit.

3. The binary hysteresis circuit of Claim 1, wherein the first adder circuit comprises a subtractor.

4. The binary hysteresis circuit of Claim 1, wherein the first adder circuit comprises an adder.

5. The binary hysteresis circuit of Claim 1, further comprising a first overflow prevention circuit coupled between the output terminal of the comparator circuit and the select terminal of the multiplexer circuit, the first overflow prevention circuit having an additional input terminal coupled to the first circuit input terminal.

6. The binary hysteresis circuit of Claim 1, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is greater than a value at the first input terminal of the comparator circuit.

7. The binary hysteresis circuit of Claim 1, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is not less than a value at the first input terminal of the comparator circuit.

8. The binary hysteresis circuit of Claim 1, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is less than a value at the first input terminal of the comparator circuit.

9. The binary hysteresis circuit of Claim 1, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is not greater than a value at the first input terminal of the comparator circuit.

10. A phase shifter circuit, comprising:

a circuit clock input terminal;

a multi-bit circuit input terminal;

a counter circuit having an input terminal coupled to the circuit clock input terminal and further having a multi-bit output terminal;

a first subtractor having a multi-bit input terminal coupled to the output terminal of the counter circuit and further having a multi-bit output terminal;

a first multiplexer circuit having a first multi-bit data input terminal coupled to the output terminal of the counter circuit, a second multi-bit data input terminal coupled to the output terminal of the first subtractor, a select terminal, and a multi-bit output terminal;

a comparator circuit having a first multi-bit input terminal coupled to the output terminal of the first multiplexer circuit, a second multi-bit input terminal coupled to the circuit input terminal, and an output terminal coupled to the select terminal of the first multiplexer circuit;

a second multiplexer circuit having a first multi-bit data input terminal coupled to the circuit input terminal, a second multi-bit data input terminal coupled to the output terminal of the counter circuit, a select terminal coupled to the output terminal of the comparator circuit, and an output terminal; and

a phase shifter having a clock input terminal coupled to the circuit clock input terminal, a multi-bit control terminal coupled to the output terminal of the second multiplexer circuit, and an output terminal.

11. The phase shifter circuit of Claim 10, further comprising a second subtractor coupled between the output terminal of the counter circuit and the first data input terminal of the first multiplexer circuit, and between the output terminal of the counter circuit and the second data input terminal of the second multiplexer circuit, wherein the second subtractor subtracts a smaller number than the first subtractor.

12. The phase shifter circuit of Claim 10, further comprising an overflow prevention circuit coupled between the output terminal of the comparator circuit and the select terminal of the first multiplexer circuit, the overflow prevention circuit having an additional input terminal coupled to the output terminal of the counter circuit.

13. The phase shifter circuit of Claim 10, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is greater than a value at the first input terminal of the comparator circuit.

14. The phase shifter circuit of Claim 10, wherein the comparator circuit is coupled to provide an indicator at the output terminal of the comparator circuit when a value at the second input terminal of the comparator circuit is not less than a value at the first input terminal of the comparator circuit.

15. A method of performing a greater-than comparison between first and second binary values while providing binary hysteresis, the method comprising:

reporting, when the second binary value increases to a value greater than the first binary value, that the second binary value is greater than the first binary value; and

continuing to report, when the second binary input value decreases to a value not greater than the first binary value, that the second binary value is greater than the first binary value until the second binary value is less than the first binary value by a predetermined constant.

16. A method of performing a less-than comparison between first and second binary values while providing binary hysteresis, the method comprising:

reporting, when the second binary value decreases to a value less than the first binary value, that the second binary value is less than the first binary value; and

continuing to report, when the second binary value increases to a value not less than the first binary value, that the second binary value is less than the first binary value until the second binary value is greater than the first binary value by a predetermined constant.

17. A method of comparing two binary values while providing binary hysteresis, the method comprising:

selecting one of first and second binary values to provide a first multi-bit value, the first and second binary values differing by a predetermined constant;

performing a comparison between the first multi-bit value and a second multi-bit value and providing a comparison output signal representing the result of the comparison; and

controlling the selecting one of the first and second binary values using the comparison output signal.

18. The method of Claim 17, wherein performing the comparison comprises determining whether the second multi-bit value is greater than the second multi-bit value.

19. The method of Claim 17, wherein performing the comparison comprises determining whether the second multi-bit value is no less than the second multi-bit value.

20. The method of Claim 17, wherein performing the comparison comprises determining whether the first multi-bit value is less than the second multi-bit value.

21. The method of Claim 17, wherein performing the comparison comprises determining whether the first multi-bit value is no greater than the second-multi-bit value.

22. The method of Claim 17, further comprising:

ensuring that the first binary value is selected when the first binary value has a predetermined value.

23. The method of Claim 22, wherein the predetermined value comprises an all-zero value.